



Attorney Docket # YOR920030292US1 (163-8)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Bhavnagarwala, et al.

Serial No.: 10/625,959

Filed: July 24, 2003

For: METHOD AND STRUCTURE FOR  
REDUCING GATE LEAKAGE AND  
THRESHOLD VOLTAGE FLUCTUATION IN  
MEMORY CELLS

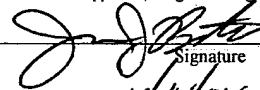
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop PGPUB Drawings, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

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James J. Bitetto

Name of applicant, assignee or Registered Representative



Signature

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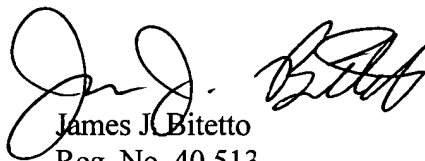
SUBMISSION OF FORMAL DRAWINGS

In accordance with 37 C.F.R. §1.84, applicant submits herewith three (3) sheets of formal drawings for the above-identified application.

Respectfully submitted,

KEUSEY, TUTUNJIAN & BITETTO, P.C.

By



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4/14/04

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